Code No: R7220404 **1**

II B.Tech. II Semester(R07) Regular Examinations,April/May 2009
SWITCHING THEORY AND LOGIC DESIGN
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks
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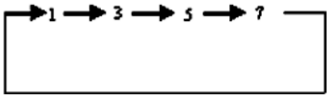
1. Convert the following numbers
   (a) $(4567)_8$to base 10.
   (b) $(11001101.0101)_2$ to base 8 and base 4.
   (c) $(53.1575)_{10}$ to base 2.
   (d) Represent +25 and -25 in sign magnitude. Sign-1's complement and sign-2's complement representation.
   (e) Why the computer works for binary number system only?
2. (a) What are universal gates? Realize AND, OR, NOT, XOR gates using universal gates.
   (b) Simplify the following Boolean function to minimum number of literals.
      i. xyz+$\bar{x}$y+xy$\bar{z}$
      ii. xy+$\bar{x}$yz
   (c) Mention the properties of XOR gate.
3. (a) Minimize the following Boolean function in SOP form and realize using NAND Gates (use k-map)
   F(A,B,C,D)= Σ m(0,1,2,3,5,7,8,9,11,14)
   (b) Minimize the following Boolean function in POS form using K-map
   F(A,B,C,D)= Π M(4,6,10,12,13,15).
4. (a) Implement the following Boolean function using
      i. 8× 1 multiplexer.
      ii. 4× 1 multiplexer.
   F(A,B,C,D)= Σm(2,5,8,9,10,14,15).
   (b) Design 4×16 decoder using two 3× 8 decoders with block diagrams.
5. (a) Explain the architecture of PLDs.
   (b) Tabulate the PLA programming table for the following Boolean functions.
   A(x,y,z)= Σ m(1,3,5,7)
   B(x,y,z)= Σ m(2,4,5,6)
   C(x,y,z)= Σ m(3,5)
6. (a) What is race-around problem in JK flip-flop? Explain how it is eliminated in Master-Slave J K flip flop.
   (b) Design Mod-6 synchronous counter using J-K flip-flops
7. (a) Compare Mealy and Moore models with block diagram.
   (b) Determine the minimal state equivalent of the state table given below.

PS	NS,Z	
	x=0	x=1
q_0	$q_0, 1$	$q_4, 0$
q_1	$q_0, 0$	$q_4, 0$
q_2	$q_1, 0$	$q_5, 0$
q_3	$q_1, 0$	$q_5, 0$
q_4	$q_2, 0$	$q_6, 1$
q_5	$q_2, 0$	$q_6, 1$
q_6	$q_3, 0$	$q_7, 1$
q_7	$q_3, 0$	$q_7, 1$

8. (a) Explain steps in designing the sequential circuit using ASM technique.
   (b) Design synchronous state machine to generate following sequence of status. Represent the machine by a state diagram 1 ASM chart and display the on set of state 7(111)with LED. Use J-K flip flops.



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Code No: R7220404 **2**

II B.Tech. II Semester(R07) Regular Examinations, April/May 2009
SWITCHING THEORY AND LOGIC DESIGN
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. (a) Convert the following numbers:
   i. $(6753)_8$ to base 10.
   ii. $(00111101.0101)_2$ base 8 and base 4.
   iii. $(95.75)_{10}$ to base 2.
   (b) Represent +65 and -65 in sign-magnitude, Sign-1's complement, Sign-2's complement representation.
   (c) Why the computer works for binary number system only?
2. (a) State and prove DeMorgan's Laws. Mention gate equivalents.
   (b) Simplify the following Boolean functions to minimum number of literates.
   i. $xy + x\bar{y}$
   ii. $(x + y)(x + \bar{y})$
   (c) Realise XOR gate using minimum number of NAND gates.
   (d) Which gate can be used as bit comparator? Why?
3. (a) Minimize the following Boolean function using K-map in SOP form and realize using NAND gates. F(A,B,C,D)= Σ m(0,1,2,3,7,8,9,10,11,12,13)
   (b) Reduce the following expression using K-map F=$\bar{B}\bar{A} + \bar{A}B + A\bar{B}$
4. (a) Implement the following Boolean function using
   i. 8×1 multiplexer.
   ii. 4×1 multiplexer. F(A,B,C,D)= M(1,5,6,9,11,14,15)
   (b) Design 2×4 decoder using NAND gates.
5. (a) Explain the capabilities and the limitations threshold gate.
   (b) Tabulate the PLA programming table for the following Boolean function.
   A(x,y,z)= $\Sigma m(0,2,3,7)$ B(x,y,z)= $\Sigma m(1,3,4,6)$ C(x,y,z)= $\Sigma m(1,4)$
6. (a) Draw the truth tables and symbols of S-R, J-K, T and D flip-flops.
   (b) Design Mod-12 synchronous counter using J-K flip-flops.
7. (a) Explain the capabilities and limitations of finite state machines.
   (b) Determine minimal state equivalent of state table given below.

PS	NS,Z	
	X=0	X=1
1	1,0	1,0
2	1,1	6,1
3	4,0	5,0
4	1,1	7,0
5	2,0	3,0
6	4,0	5,0
7	2,0	3,0

8. (a) Explain salient features of ASM chart.
   (b) Draw the state diagram and ASM chart for 2bit up-down counter having mode control input M=0 Down counting, M=1 up counting. The circuit should generate a output whenever count becomes minimum or maximum.

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Code No: R7220404 **3**

II B.Tech. II Semester(R07) Regular Examinations, April/May 2009
SWITCHING THEORY AND LOGIC DESIGN
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks
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1. (a) Convert following numbers:
   i. $(11010011.1100)_2$ to hexa decimal.
   ii. $(425.125)_{10}$ to base 5.
   iii. $(123)_4$ to decimal.
   (b) Represent +45 and -45 in sign-magnitude. Sign-1's complement sign -2's complement, representation.
   (c) Why the computer works for binary number system only?
2. (a) State and prove Boolean laws related to OR, AND, NOT gates.
   (b) Find the complement of the following functions:
   i. $F_1 = \bar{x}y\bar{z} + \bar{x}\bar{y}z$
   ii. $F_2 = x(\bar{y}\bar{z} + yz)$
   (c) Realize XOR gate using minimum number of NAND gates
3. (a) Minimize the following Boolean function using K-map in SOP form and realize using NAND gates.
   F(A,B,C,D)= Σ m(1,3,5,8,9,11,15)+ d(2,13)
   (b) Find output of 4 variable K map when the minterns 0 to 3 and 8 to 11 are filled with Logic HIGH.
4. (a) Implement the following Boolean function using 8×1 multiplexer
   F(A,B,C,D)= Σ m(0,2,4,6,8,10,12,14)
   (b) What is encoder? Design octal to binary encoder.
5. (a) Explain the architecture of PLDs.
   (b) Construct 128 × 8 ROM using 32×8 ROM.
6. (a) Compare synchronous and Asynchronous circuits
   (b) Design Mod-12 synchronous counter using J-K flip flops.
7. (a) Explain state minimization procedure.
   (b) Determine minimal state equivalent of state table given below.

PS	NS,Z	
	x=0	x=1
q_0	$q_0, 1$	$q_4, 0$
q_1	$q_0, 0$	$q_4, 0$
q_2	$q_1, 0$	$q_5, 0$
q_3	$q_1, 0$	$q_5, 0$
q_4	$q_2, 0$	$q_6, 1$
q_5	$q_2, 0$	$q_6, 1$
q_6	$q_3, 0$	$q_7, 1$
q_7	$q_3, 0$	$q_7, 1$

8. (a) Explain steps in designing the sequential circuit using ASM technique.
   (b) Draw the state diagram and ASM chart for 2 bit up-down counter having mode control input:
   m=0 Down counting
   m=1 Up counting
   The circuit should generate a output 1 whenever count becomes minimum or maximum

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Code No: R7220404 **4**

II B.Tech. II Semester(R07) Regular Examinations,April/May 2009
SWITCHING THEORY AND LOGIC DESIGN
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. (a) Convert the following numbers.
   i. (11010111.110)to octal and hexa.
   ii. (125.25) to base 4 and base 8.
   (b) Represent +35 and -35 in sign magnitude, Sign-1's complement and sign-2's complement representation.
   (c) Why the computer works for binary number system only?
2. (a) State the prove the following Boolean laws:
   i. Commutative.
   ii. Associative.
   iii. Distributive.
   (b) Simplify the following Boolean function to minimum number of literals
   i. $\overline{(a+b)}.\overline{(\bar{a}+\bar{b})}$
   ii. $y(w\bar{z}+wz)+xy$
   (c) Realize XOR gate using minimum number of NAND gates.
3. (a) Minimize the following Boolean function using k-map in SOP form and realize using NAND gates. F(A,B,C,D)= Σm(1,3,7,11,15)+ d(0,2,5)
   (b) What is meant by pair, quad and octet of k-map and how many variables are eliminated in each. Demonstrate with examples.
4. (a) Implement the following Boolean function using 8×1 multiplexer F(A,B,C,D)=Σm(0,1,3,4,8,9,15)
   (b) What is encoder? Design decimal to BCD encoder.
5. (a) Explain capabilities and limitations of threshold gates.
   (b) Construct 128×8 ROM using 32 × 8 ROM chips.
6. (a) Derive the circuit table of J-K flip flop using circuit diagram
   (b) Design Mod-10 synchronous counter using J-K flip flops
7. (a) Compare Mealy and More models with block diagram
   (b) Determine minima state equivalent of the state table shown below.

PS	NS,Z	
	X=0	X=1
1	1,0	1,0
2	1,1	6,1
3	4,0	5,0
4	1,1	7,0
5	2,0	3,0
6	4,0	5,0
7	2,0	3,0

8. (a) Explain the salient features of ASM chart.
   (b) Draw the state diagram and ASM chart for 2bit up-down counter having mode control input.
   M=1 up counting
   M=0 Down counting
   The circuit should generate a output 1, when ever count below minimum or maximum

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